IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Leonard Forbes et al.

Title: CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

Docket No.: 303.378US1

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(NEW FILING)

Carburized Silicon Gate Insulators for Integrated Circuits

Field of the Invention

The present invention relates to semiconductor field effect transistors, and in particular to insulators for gates of field effect transistors.

Background of the Invention

Field-effect transistors (FETs) are typically produced using a standard complementary metal-oxide-semiconductor (CMOS) integrated circuit fabrication process. As is well known in the art, such a process allows a high degree of integration such that a high circuit density can be obtained with the use of relatively few well-established masking and processing steps. A standard CMOS process is typically used to fabricate FETs that each have a gate electrode that is composed of n-type conductively doped polycrystalline silicon (polysilicon) material or other conductive materials.

Field effect transistors (FETs) are used in many different types of memory devices, including EPROM, EEPROM, EAPROM, DRAM and flash memory devices. They are used as both access transistors, and as memory elements in flash memory devices. In these applications, the gate is electrically isolated from other conductive areas of the transistor by an oxide layer. A drawback with FETs having grown oxide insulators is manifested in the use of Fowler-Nordheim tunneling to implement nonvolatile storage devices, such as in electrically erasable and programmable read only memories (EEPROMs). EEPROM memory cells typically use CMOS floating gate FETs. A floating gate FET typically includes a floating (electrically isolated) gate that controls conduction between source and drain regions of the FET. In such memory cells, data is represented by charge stored on the floating gates. Fowler-Nordheim tunneling is one method that is used to store charge on the floating gates during a write operation and to remove charge from the polysilicon floating gate during an erase

operation. The high tunneling voltage of grown oxides used to provide such isolation increases the time needed to store charge on the floating gates during the write operation and the time needed to remove charge from the polysilicon floating gate during the erase operation. This is particularly problematic for "flash" EEPROMs, which have an architecture that allows the simultaneous erasure of many floating gate transistor memory cells. Since more charge must be removed from the many floating gates in a flash EEPROM, even longer erasure times are needed to accomplish this simultaneous erasure. There is a need in the art to obtain floating gate transistors allowing faster storage and erasure, such as for use in flash EEPROMs.

Many gate insulators have been tried, such as grown oxides, CVD (chemical vapor deposition) oxides, and deposited layers of silicon nitride, aluminum oxide, tantalum oxide, and titanium oxide with or without grown oxides underneath. The only commonly used gate insulator at the present time is thermally grown silicon oxide. If other insulators are deposited directly on the silicon, high surface state densities result. Composite layers of different insulators are first grown and then deposited, such as oxide-CVD oxide or oxide-CVD nitride combinations. If composite insulators are used, charging at the interface between the insulators results due to trap states at this interface, a bandgap discontinuity, and/or differences in conductivity of the films.

There is a need for a gate insulator which provides a low tunneling barrier. There is a further need to reduce the tunneling time to speed up storage and retrieval of data in memory devices. There is yet a further need for a gate insulator with less charging at the interface between composite insulator layers. A further need exists to form gate insulators with low surface state densities.

Summary of the Invention

Silicon carbide films are grown by carburization of silicon to form insulative films. In one embodiment, the film is used to provide a gate insulator for a field effect transistor. The film is grown in a microwave-plasma-enhanced chemical vapor deposition (MPECVD) system. A silicon substrate is first etched in dilute HF solution

and rinsed. The substrate is then placed in a reactor chamber of the MPECVD system in hydrogen along with a carbon containing gas. The substrate is then inserted into a microwave generated plasma for a desired time to grow the film. The microwave power varies depending on substrate size.

The resulting SiC film is preferably amorphous and has low surface state densities. It provides a gate insulator having a much lower tunneling barrier as compared to grown oxides which are widely used today. The lower tunneling barrier results in reduced tunneling times and allows reduction of power supply voltages. Further, charging at interfaces between composite insulators is reduced.

Methane, and other carbon containing gases having from about one to ten carbon atoms per molecule may be used. The temperature of the system may vary between approximately 915 degrees C to 1250 degrees C, with films growing faster at higher temperatures. Thicknesses of the resulting film range from 2 nm in a time period as short as 3 minutes, to as thick as 4500 Angstrom in one hour. The thicker films require longer time and higher temperature since the formation of SiC is a diffusion limited process.

The growth of the film may be continued following formation of an initial film via the above process by using a standard CVD deposition of amorphous SiC to form a composite insulator. The film may be used to form gate insulators for flash type memories as well as gate insulators for CMOS and MOS transistors used in semiconductors such as DRAMs. Further, since SiC has a fairly high dielectric constant, it may be formed as dielectric layers in capacitors in the same manner. It can also be used to form gate insulators for photo sensitive FETs for imaging arrays.

Brief Description of the Drawings

Figure 1 is a cross-sectional view, illustrating one embodiment of a transistor according to one aspect of the invention, including a grown silicon carbide (SiC) gate insulator.

Figure 2 is a cross-sectional view, illustrating one embodiment of a transistor according to one aspect of the invention, including a grown silicon carbide (SiC) gate insulator.

Figure 3 is a cross-sectional view, illustrating one embodiment of a capacitor according to one aspect of the invention, including a grown silicon carbide (SiC) dielectric.

Figure 4 is a simplified block diagram illustrating generally one embodiment of a memory system incorporating grown SiC gate insulated FETs according to one aspect of the present invention.

Figure 5 is a simplified block circuit diagram of an imaging device employing photo sensitive transistors having grown SiC gate insulators.

Attorney Docket No. 1303.009US1

Description of the Embodiments

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. The terms wafer and substrate used in the following description include any semiconductor-based structure having an exposed surface with which to form the integrated circuit structure of the invention. Wafer and substrate are used interchangeably to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Figure 1 is a cross-sectional view illustrating generally, by way of example, one embodiment of a n-channel FET provided by the invention. The FET includes a source region 102, a drain region 104 and a gate region 106. In one embodiment, source 102 and drain 104 are fabricated by forming regions of highly doped (n+) regions in a lightly doped (p-) silicon semiconductor substrate 108. In another embodiment, substrate 108 includes a thin semiconductor surface layer formed on an underlying insulating portion, such as in a SOI or other thin film transistor process technology. Source 102 and drain 104 are separated by a predetermined length in which a channel region 110 is formed.

In one embodiment, for example, layer 112 is a polysilicon control gate in a floating gate transistor in an electrically erasable and programmable read-only memory (EEPROM) memory cell. In this embodiment, gate 106 is floating (electrically isolated) for charge storage thereupon, such as by known EEPROM techniques. In another embodiment, for example, layer 112 is, a metal or other conductive interconnection line that is located above gate 106.

The upper layers, such as layer 112 can be covered with a layer 116 of a suitable insulating material in the conventional manner, such as for isolating and protecting the physical integrity of the underlying features. Gate 106 is isolated from channel 110 by an insulating layer 118, which is formed of carburized silicon, SiC.

SiC is a wide bandgap semiconductor material with a bandgap energy of about 2.1 eV. Moreover, SiC has an electron affinity of about 3.7 to 3.8 eV, in contrast to silicon, which has an electron affinity of about 4.2 eV. The smaller electron affinity of the SiC gate 106 material reduces the tunneling barrier potential which reduces the tunneling distance and increases the tunneling probability. This speeds the write and erase operations of storing and removing charge by Fowler-Nordheim tunneling to and from the gate 106, which is a floating gate. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously. The large charge that must be transported by Fowler-Nordheim tunneling during the erasure of a flash EEPROM typically results in relatively long

erasure times. By reducing the tunneling distance and increasing the tunneling probability, the SiC insulating layer 118 reduces erasure times in flash EEPROMs.

In one embodiment, the SiC layer 118 is grown in a microwave-plasma-enhanced chemical vapor deposition (MPECVD) system. A silicon substrate is first etched in dilute HF for about one minute and thoroughly rinsed in deionized water prior to insertion into a reactor, such as an Applied Materials single wafer system, model number 5000, which has four to five process chambers, each holding one wafer. Following insertion in the chamber, the chamber is first evacuated to a pressure of 10^{-4} or 10^{-5} mTorr. Carburization of silicon is then performed in a 2% to about 10% concentration of CH_4/H_2 with a chamber pressure of approximately 25 to 15 Torr depending upon the reactor configuration, horizontal or vertical. Typical microwave power is 1,000 watts for an 8 to 10 inch wafer to 250 to 300 watts for 3 to 4 inch wafers. The substrate is immersed roughly 0.5 cm into a resulting plasma. The temperature when the wafer is inserted into the reactor is typically about 400 to 500 degrees C, and is quickly ramped up to about 915 to 1250 degrees C to carburize the silicon. The higher the temperature and concentration of methane in hydrogen, the faster the film growth. In further embodiments, an electrical bias of between zero and 200 volts may be applied during the carburization.

Besides methane and hydrogen mixtures, other carbon-containing gases may also be used, including those selected from the group consisting of ethane, ethylene, acetylene, ethanol, and other hydrocarbons with from about one to ten carbon atoms per molecule. Thicker, composite layers can also be formed by chemical vapor deposition CVD of amorphous SiC after an initial carburized silicon layer is formed.

Layers of SiC grown in the above manner are highly amorphous. The risk of obtaining undesired microcrystalline inclusions is greatly reduced. In addition, much lower surface state densities are obtained over deposition techniques, resulting in improved FET performance.

In one example, at 915 degrees C with a 2% concentration of CH_4/H_2, a 2nm film of SiC may be grown in about three minutes.

In a second example, at 1250 degrees C with 4% concentration of CH_4/H_2, a 4500 Angstrom thickness film can be grown in about one hour.

Figure 2 is a cross-sectional view illustrating generally, by way of example, one embodiment of a partially formed n-channel FET provided by the invention. The FET includes a source region 202, a drain region 204 and a gate region 206. In one embodiment, source 202 and drain 204 are fabricated by forming regions of highly doped (n+) regions in a lightly doped (p-) silicon semiconductor substrate 208. In another embodiment, substrate 208 includes a thin semiconductor surface layer formed on an underlying insulating portion, such as in a SOI or other thin film transistor process technology. Source 202 and drain 204 are separated by a predetermined length in which a channel region 210 is formed. Gate 206 is isolated from channel 210 by an insulating layer 218, which is formed of carburized silicon, SiC formed as described above.

Figure 3 is a schematic cross-sectional view of a semiconductor wafer generally illustrating a portion of a DRAM cell formed on and in the surface of a substrate 320. Thick field oxide regions 322 are selectively formed around active area regions in which memory access transistors are to be created, completely enclosing these active area regions along the surface of the wafer. The insulating thick field-oxide regions 322 isolate transistors such as memory access transistor from each other. Word lines 324a, 324b, 324c, collectively 324, have been formed on both active area regions and on field oxide regions 322. Each word line 324 serves as common gate for multiple memory access transistors. Each word line 324 has multiple stacked layers, such as: a thin carburized silicon (gate insulator) layer 325 most proximate to substrate 320; a conductive layer such as a doped polysilicon on the gate insulator layer; a silicide layer such as tungsten silicide, tantalum silicide, or titanium silicide on the conductive layer; and, an insulator on the silicide layer. In Figure 3, the multiple stacked layers of each word line 324 are illustrated generally as only two layers: the top insulator layer, and the underlying stacked structure described above. A first insulating layer 328 acts as an etch-stop to protect underlying topography during further processing steps. The first

insulating layer 328 is preferably composed of silicon nitride (nitride), but other layers of materials or combinations of layers of materials with suitable etch-stop properties may also be used.

A relatively thick second insulating layer 330 is conformally deposited, preferably by CVD, on the first insulating layer 328. The surface topography of second insulating layer 330 is minimized by planarization, preferably by chemical-mechanical polishing (CMP). The second insulating layer 330 is composed of borophosphosilicate glass (BPSG) or material compatible with use of the first insulating layer 328 as an etch-stop, such as phosphosilicate glass (PSG). The etch rate of second insulating layer 330 should be substantially greater than the etch rate of first insulating layer 328. Minimizing the topography of second insulating layer 330 by CMP planarization results in a relatively flat surface for subsequent processing steps.

The second insulating layer 330 is selectively patterned to define a buried contact opening 332. Buried contact opening 332 is anisotropically etched through second insulating layer 330 and through portions of the underlying first insulating layer 328. This anisotropic etching forms sidewall spacers 331 from first insulating layer 328. The formation of sidewall spacers 331 results from a greater vertical thickness of first insulating layer 328 in the regions adjacent to and contacting the word lines 324 than in the other anisotropically etched regions.

A source/drain diffusion 326b is formed within buried contact opening 332. In one embodiment, source/drain diffusion 326b is formed by ion-implantation of dopants into the substrate 320. Ion-implantation range of the dopants is limited by the sidewall spacers 331 and field oxide 322. Second insulating layer 330, buried contact opening 332 and word lines 324b, 324c contained within buried contact opening 332 provide topography used as a form during the conformal deposition of a thin conductive bottom plate layer 334. The conductive bottom plate layer 334 physically and electrically contacts the surface of source/drain diffusion 326b within buried contact opening 332. In one embodiment, dopants from the conductive bottom plate layer 334 are diffused by thermal processing steps into source/drain diffusion 326b, augmenting the dopant

concentration of source/drain diffusion 326b. The conformal deposition of conductive bottom plate layer 334 is preferably by CVD of in situ doped or separately doped polysilicon. Hemispheric grained polysilicon may also be used to increase the surface area of conductive bottom plate layer 334.

Portions of the conductive bottom plate layer 334 which are outside the buried contact opening 332 are removed, preferably by CMP planarization, thereby exposing the second insulating layer 330. After CMP planarization, a thin layer 338 of silicon is conformally deposited on the remaining portions of the conductive bottom plate layer 334 within buried contact opening 332 and on the exposed portions of the second insulating layer 330. The thin silicon layer 338 is then carburized in the manner described above to become a thin dielectric layer 338. Further thickness may again be added by CVD deposition of amorphous SiC after the initial layer is grown. A conductive top plate layer 340, preferably polysilicon, is conformally deposited on the thin dielectric layer 338. The conformal deposition of conductive top plate layer 340 is preferably by CVD of in situ doped or separately doped polysilicon. Use of grown SiC for a capacitor dielectric avoids difficulties in working with other high dielectric constant materials, and provides a good dielectric for low voltage applications.

Figure 4 is a simplified block diagram illustrating generally one embodiment of a memory 400 system incorporating SiC gate insulator FETs according to one aspect of the present invention. The SiC gate insulator FETs are used in various applications within memory 400 including, for example, in logic and output driver circuits. The SiC gate insulator FETs can also function as memory cell access FETs, such as in a dynamic random access memory (DRAM) embodiment of memory 400, or as other memory elements therein. In one embodiment, memory 400 is a flash EEPROM, and the SiC gate FETs are floating gate transistors that are used for nonvolatile storage of data as charge on the SiC floating gates. However, the SiC gate FETs can also be used in other types of memory systems, including SDRAM, SLDRAM and RDRAM devices, or in programmable logic arrays (PLAs), or in any other application in which transistors are used.

Flash EEPROM memory 400 comprises a memory array 402 of multiple memory cells. Row decoder 404 and column decoder 406 decode addresses provided on address lines 408 to access addressed SiC isolated floating gate transistors in the memory cells in memory array 402. Command and control circuitry 410 controls the operation of memory 400 in response to control signals received on control lines 416 from a processor 401 or other memory controller during read, write, and erase operations. Data is transferred between the memory 400 and the processor 401 via data lines 418.

As described above, the floating SiC isolation layers of the floating gate transistors in memory array 402 advantageously reduce the tunneling distance and increase the tunneling probabilities, thereby speeding write and erase operations of memory 400. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously, which normally results in relatively long erasure times. By reducing the tunneling distance and increasing the tunneling probability, charge is more easily transferred to and from the SiC isolated floating gates, thereby reducing erasure times in flash EEPROMs.

In a further embodiment, an array of floating gate transistors 510 is used in an imaging device shown in simplified block form generally at 512 in Figure 5. In essence, the imaging device comprises an array of floating gate transistors having SiC isolated floating gates. The transistors are arranged in a symmetrical homogenous layout corresponding to image pixels. They are formed to allow light to penetrate to the gates. Light, incident on the gates has a significant photoelectric effect due to the reduced barrier height to cause the discharge of electrons stored on the floating gates. The use of a SiC grown layer gate insulator advantageously reduces the barrier height and increases photoelectric emission over the barrier, making such transistors much more responsive to light than prior transistors using prior grown gate oxides. Access lines 514, 516 are respectively coupled to the source and control or programming gates of each transistor to read the remaining charge following exposure to light, and to recharge the transistor gates prior to further exposures in a manner consistent with other

such devices. The access lines 514, 516 are also coupled to row and column decoder circuitry such as that shown in Figure 4. In one embodiment, the array 512 may be substituted for array 402 in Figure 4, and the decoder and control circuitry is used to read and reset the transistors 510.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description without departing from the scope of the present invention.

What is claimed is:

1. An integrated circuit field effect transistor having an amorphous carburized silicon layer gate insulator.

2. An integrated circuit field effect transistor comprising:

a source and a drain separated by a channel supported by a semiconductor substrate;

a gate supported by the substrate and extending between the source and drain above the channel; and

an insulative amorphous layer of carburized silicon formed between the channel and the gate.

3. An integrated circuit memory device supported by a semiconductor substrate, the device comprising:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate supported by the substrate and extending between the source and drain above the channel;

a control gate formed adjacent to and insulated from the floating gate; and

an insulative layer of carburized silicon formed between the channel and the gate.

4. An integrated circuit capacitor supported by a semiconductor substrate, the capacitor comprising:

a first conductor layer supported by the substrate;

a dielectric layer of carburized silicon formed on top of the first conductor layer; and

a second conductor layer formed on top of the dielectric layer.

5. The capacitor of claim 4 wherein at least part of the layers extend substantially vertically from a general surface of the substrate.

6. The capacitor of claim 4 wherein the capacitor is part of a memory cell, and the layers are formed at least partially over memory cell access circuitry.

7. A memory device comprising:

an array of memory cells having capacitors that store charges representative of data and have access transistors formed with carburized silicon gate insulators;

decode circuitry coupled to the array; and

control circuitry coupled to the decode circuitry and the array of memory cells.

8. A semiconductor memory device comprising:

a memory array including a plurality of transistors, each of the transistors including a source region, a drain region, a conductive channel separating the source and drain regions, and an electrically isolated floating gate located adjacent the channel and separated therefrom by a layer of carburized silicon insulating material, and a control gate located proximal to the floating gate and separated therefrom by a layer of insulating material;

addressing circuitry for addressing the memory array; and

control circuitry for controlling read, write, and erase operations of the memory device.

9. An imaging device comprising:

an array of light sensitive carburized silicon floating gate transistors that store charges on the floating gate and discharge responsive to light;

decode circuitry coupled to the array; and

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control circuitry coupled to the decode circuitry and the array of floating gate transistors.

10. A method of forming a gate insulator for a semiconductor device comprising the steps of:

cleaning a silicon substrate;

growing a layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing environment.

11. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrogen and hydrocarbon gas which contains from about 1 to 10 carbon atoms per molecule;

forming the gate on top of the SiC layer; and

forming a source and drain.

12. The method of claim 11 wherein the hydrocarbon gas comprises at least one of methane, ethane, ethylene, acetylene, and ethanol.

13. The method of claim 11 wherein the concentration of hydrocarbon gas in hydrogen is between approximately 2% to 10%.

14. The method of claim 11 wherein the layer of SiC is grown in a pressure of between approximately 15 to 25 Torr.

15. The method of claim 11 and further comprising the step of forming a second SiC layer by chemical vapor deposition of amorphous SiC after growing the first layer and prior to forming the gate.

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16. The method of claim 11 wherein a microwave power of between approximately 250 to 1000 watts is used while growing the first SiC layer.

17. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber in a 2 to 10% concentration of a hydrocarbon gas which contains from about 1 to 10 carbon atoms per molecule in hydrogen at a pressure of between approximately 15 to 25 Torr;

forming the gate on top of the SiC layer; and

forming a source and drain.

18. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber at a microwave power of between approximately 250 to 1000 watts in a hydrocarbon gas which contains from about 1 to 10 carbon atoms per molecule in hydrogen;

forming the gate on top of the SiC layer;

forming a source and drain; and

growing a second SiC layer by chemical vapor deposition of amorphous SiC after growing the first layer and prior to forming the gate.

19. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber at a microwave power of between approximately 250 to 1000 watts in a 2 to 10% concentration of a hydrocarbon gas which

contains from about 1 to 10 carbon atoms per molecule in hydrogen at a pressure of between approximately 15 to 25 Torr;

forming the gate on top of the SiC layer;

forming a source and drain; and

growing a second SiC layer by chemical vapor deposition of amorphous SiC after growing the first layer and prior to forming the gate.

Abstract of the Disclosure

Silicon carbide films are grown by carburization of silicon to form insulative films. In one embodiment, the film is used to provide a gate insulator for a field effect transistor. The film is grown in a microwave-plasma-enhanced chemical vapor deposition (MPECVD) system. A silicon substrate is first etched in dilute HF solution and rinsed. The substrate is then placed in a reactor chamber of the MPECVD system in hydrogen along with a carbon containing gas. The substrate is then inserted into a microwave generated plasma for a desired time to grow the film. The microwave power varies depending on substrate size. The growth of the film may be continued following formation of an initial film via the above process by using a standard CVD deposition of amorphous SiC. The film may be used to form gate insulators for FET transistors in DRAM devices and flash type memories. It may be formed as dielectric layers in capacitors in the same manner.

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Matthew Hollister
(Name)

(Signature) 7-29-97
(date)

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

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The specification of which is attached hereto.

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Kie Y. Ahn

Full Name of inventor:
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Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

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(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

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(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

☐ I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

☐ I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

☐ I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No. 39,610	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Billig, Patrick G.	Reg. No. 38,080	Forrest, Bradley A.	Reg. No. 30,837	Lynch, Michael L.	Reg. No. 30,871
Billion, Richard E.	Reg. No. 32,836	Harris, Robert J.	Reg. No. 37,346	Pappas, Lia M.	Reg. No. 34,095
Brennan, Thomas F.	Reg. No. 35,075	Holloway, Sheryl S.	Reg. No. 37,850	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Klima-Silberg, Catherine I.	Reg. No. 40,052	Simboli, Paul B.	Reg. No. 38,616
Dryja, Michael A.	Reg. No. 39,662	Kluth, Daniel J.	Reg. No. 32,146	Slifer, Russell D.	Reg. No. 39,838
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198	Viksnins, Ann S.	Reg. No. 37,748
Farney, W. Bryan	Reg. No. 32,651	Litman, Mark A.	Reg. No. 26,390	Woessner, Warren D.	Reg. No. 30,440

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Leonard Forbes**
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Corvallis, OR 97330

Signature: _____ Date: 30 June 97
Leonard Forbes

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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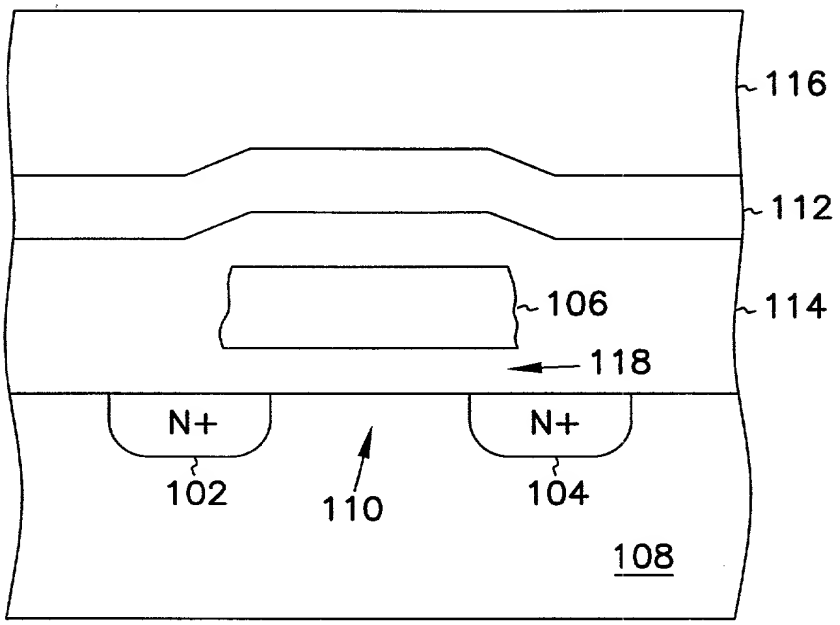

FIG. 1

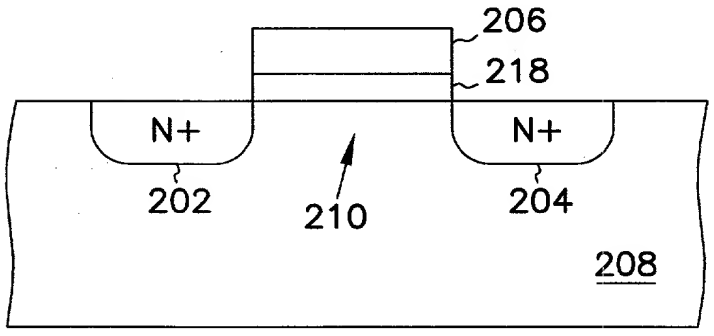

FIG. 2

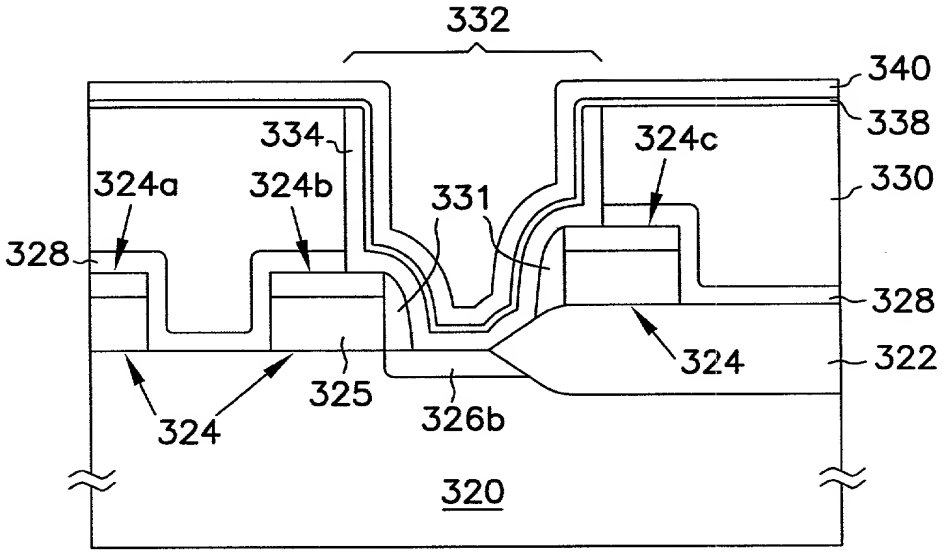
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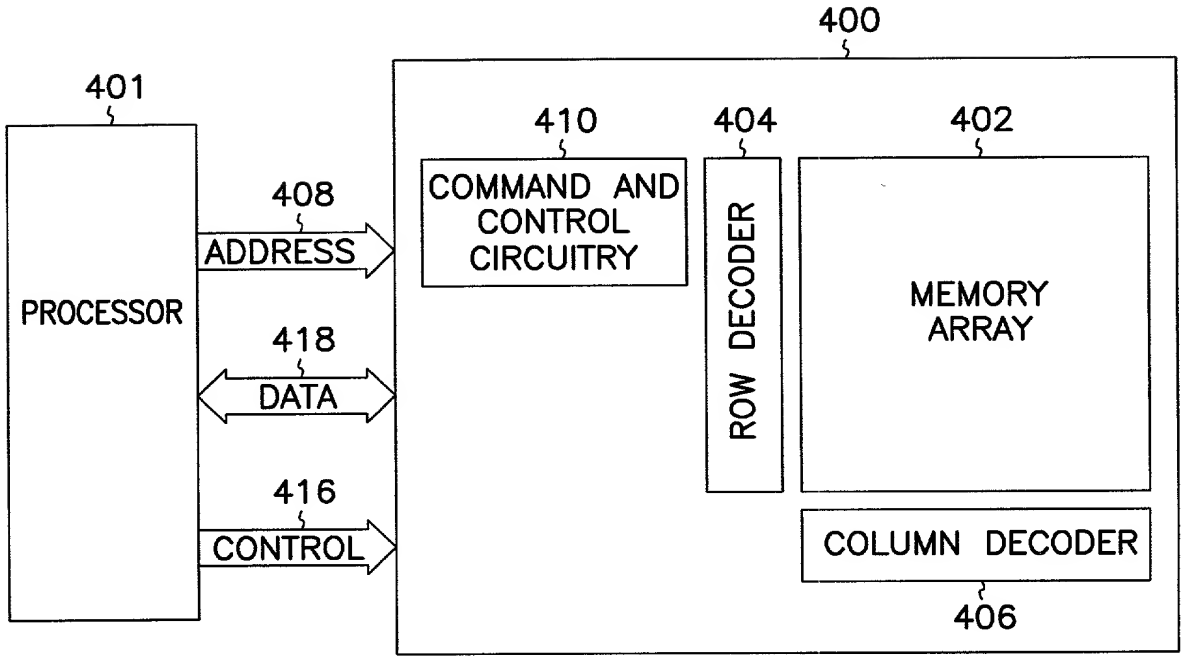
FIG. 3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401
410
404
402
COMMAND AND CONTROL CIRCUITRY
ROW DECODER
MEMORY ARRAY
PROCESSOR
408
ADDRESS
418
DATA
416
CONTROL
COLUMN DECODER
406

FIG. 4

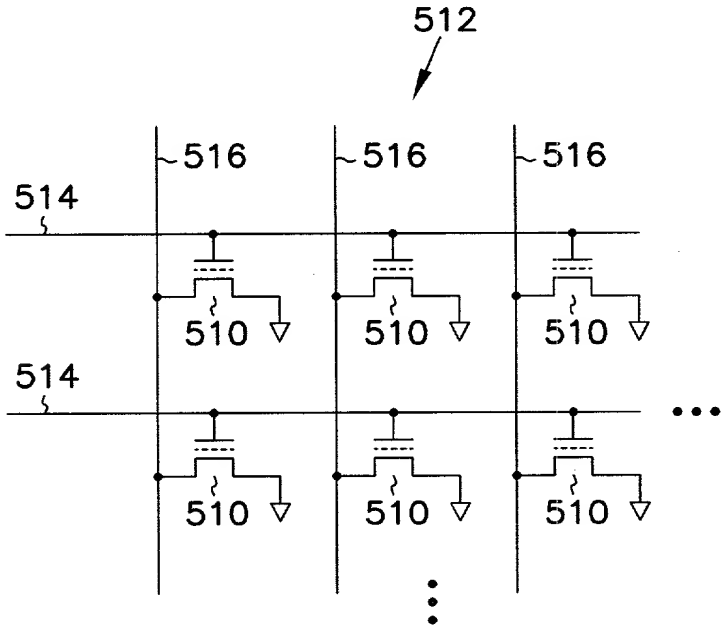
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FIG. 5